NI 6122/6123 Specifications

This document lists the I/O terminal summary and specifications for the NI 6122/6123.

For the most current edition of this document, refer to `ni.com/manuals`. Refer to the *DAQ Quick Start Guide* for more information about accessing documents on the NI-DAQ CD.

Note With NI-DAQmx, National Instruments has revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ terminal names and their NI-DAQmx equivalents, refer to the *Terminal Name Equivalents* table in the *S Series Help*.

Table 1. I/O Terminal Summary

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AI <0..7>	AI	100 MΩ in parallel with 10 pF	35/25	—	—	—	±16 nA ±35 nA
AI GND	—	—	—	—	—	—	—
D GND	—	—	—	—	—	—	—
+5 V	—	0.1 Ω 0.45 Ω	Short-circuit to ground	1 A	—	—	—
P0.<0..7>	DIO	—	V_{CC} + 0.5	13 at (V_{CC} – 0.4)	24 at 0.4	1.1	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 0/ AI START TRIG	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 1/ AI REF TRIG	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 2	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu

Table 1. I/O Terminal Summary (Continued)

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI 3/ CTR 1 SOURCE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 4/ CTR 1 GATE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 1 OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 5	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 6	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 7/ AI SAMP CLK	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 8/ CTR 0 SOURCE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 9/ CTR 0 GATE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 0 OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output DO = Digital Output pu = pull-up

Note: The tolerance on the 50 kΩ pull-up resistors is large. Actual value might range between 17 kΩ and 100 kΩ.

Specifications

The following specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

NI 6122.....4

NI 6123.....8

Type of ADC

Resolution.....16 bits, 1 in 65,536

Pipeline.....0

Sampling rate

Maximum ..... 500 kS/s per channel

Minimum ..... No minimum

Input impedance

AI – to AI GND ..... 100 MΩ in parallel with 10 pF

AI + to AI GND ..... 100 MΩ in parallel with 10 pF

Input bias current ..... ±2 pA typ, ±25 pA max

Input offset current ..... ±1 pA typ, ±10 pA max

Input coupling ..... DC

Max working voltage for all analog input channels

Positive input (AI +) ..... ±11 V for all ranges, Measurement Category I

Negative input (AI –) ..... ±11 V for all ranges, Measurement Category I

Caution Do not use for measurements within Categories II, III, or IV.

Overvoltage protection (AI +, AI –) ..... ±36 V

Input current during overvoltage conditions ..... ±20 mA max

Input FIFO size

NI 6122 ..... 16 MS

NI 6123 ..... 16 or 32 MS

Data transfers ..... DMA, interrupts, programmed I/O

DMA mode ..... Scatter-gather

DC Transfer Characteristics

INL ..... ±2 LSB max

DNL ..... –1 min, 1.5 max, no missing codes

Absolute Accuracy

Nominal Range at Full Scale (V)	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (μVrms)	Absolute Accuracy at Full Scale[1] (μV)	Sensitivity[2] (μV)
±10	123	25	5	40	186	62	330	4960	132.0
±5	123	25	5	48	192	62	166	2550	66.4
±2.5	128	25	5	52	229	62	105	1400	42.0
±1.25	128	25	5	58	251	62	60	740	24.0

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

$$\text{NoiseUncertainty} = \frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$$ For a coverage factor of 3 σ and averaging 100 points.

[1] Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 123 ppm + 25 ppm · 1 + 5 ppm · 10 GainError = 198 ppm

OffsetError = 40 ppm + 186 ppm · 1 + 62 ppm OffsetError = 288 ppm

$$\text{NoiseUncertainty} = \frac{330\ \mu\text{V} \cdot 3}{\sqrt{100}}$$ NoiseUncertainty = 99 μV

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 4960 μV

[2] Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Dynamic Characteristics

Phase mismatch..... ±0.1° at 100 kHz

Table 2. NI 6122/6123 Analog Input Dynamic Characteristics

Input Range	Bandwidth[1] (kHz)	SFDR Typ[2] (dB)	CMRR[3] (dB)	System Noise[4] (LSB_{rms})	Crosstalk[5] (dB)	THD (dB at 10 kHz)
±10 V	511	104	70	1.08	–74	–102
±5 V	511	105	70	1.09	–74	–103
±2.5 V	505	101	70	1.37	–74	–102
±1.25 V	505	101	70	1.58	–74	–101

[1] –3 dB frequency for input amplitude at 10% of the input range (–20 dB)
[2] Measured at 10 kHz with twelfth-order bandpass filter after signal source
[3] DC to 60 Hz
[4] LSB_{rms}, including quantization
[5] DC to 100 kHz

Stability

Recommended warm-up time ..... 15 min

Calibration

Calibration interval ..... 2 years

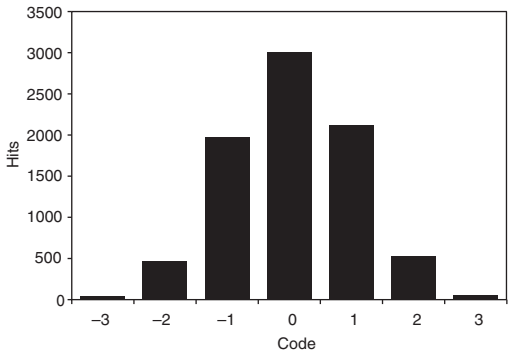
Level..... 5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient ..... ±5.0 ppm/°C max

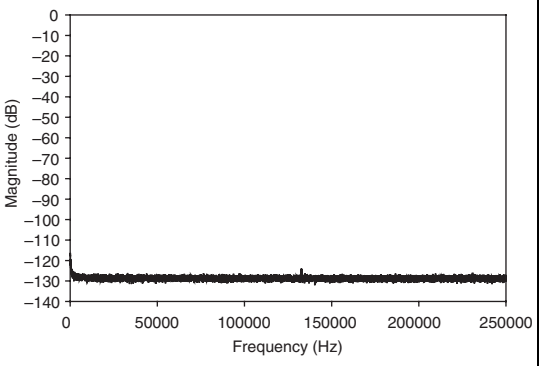
Long-term stability..... ±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Typical Performance Graphs

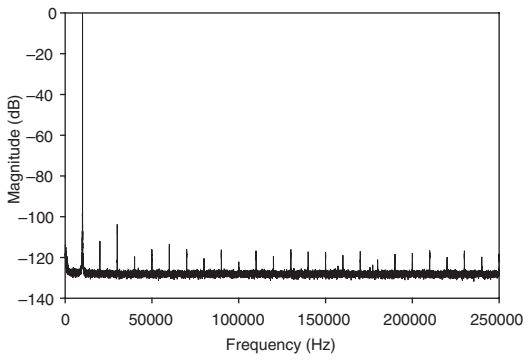
Grounded-Input Histogram



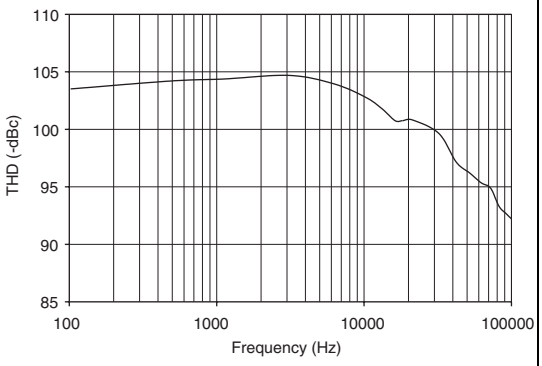
Grounded Input



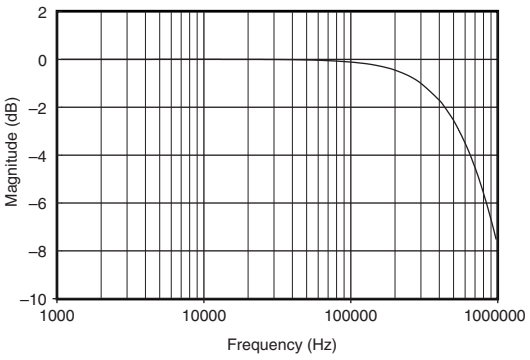
Power spectrum, 10 Vpp 100 kHz



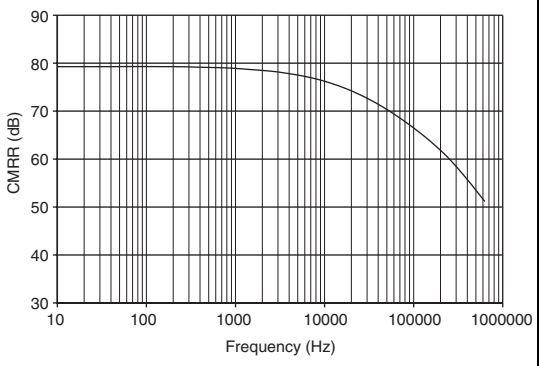
THD



Bandwidth



CMRR



Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Table 3. Digital Logic Levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... Input (high-impedance)

Data transfers ..... DMA, interrupts, programmed I/O

Input buffer ..... 2,044 bytes

Output buffer ..... 2,044 bytes

Transfer rate (1 word = 8 bits) ..... 10 Mwords/s

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers .....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather

Triggers

Analog Trigger

Source .....All analog input channels

Level .....± full-scale

Slope .....Positive or negative (software-selectable)

Resolution .....8 bits, 1 in 256

Hysteresis.....Programmable

Bandwidth (–3 dB) .....5 MHz internal/external

Digital Trigger

Compatibility .....TTL

Response .....Rising or falling edge

Pulse width .....10 ns min

RTSI Trigger Lines (PCI Only)

Trigger lines <0..6> 7

RTSI clock 1

PXI Trigger Bus (PXI Only)

Trigger lines <0..6> 7

Star trigger 1

Bus Interface

Type .....Master, slave

Power Requirement

+5 VDC (±5%)

NI 6122 ..... 1.03 A

NI 6123 ..... 1.9 A

+3.3 V

NI 6122 ..... 1.1 A

NI 6123 ..... 1.55 A

–12 V

NI 6122 ..... 52 mA

NI 6123 ..... 81 mA

Power available at I/O connector ..... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions (not including connectors)

NI PCI-6122/6123..... 31.2 × 10.6 cm (12.3 × 4.2 in.)

NI PXI-6122/6123 ..... 16.0 cm × 10.0 cm (6.3 × 3.9 in.)

I/O connector..... 68-pin male SCSI-II type

Environmental

Operating temperature..... 0 to 50 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 m

Pollution Degree (indoor use only)..... 2

Safety

The NI 6122/6123 devices are designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity	EN 61326:1997 + A2:2001, Table 1
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety)	73/23/EEC
Electromagnetic Compatibility Directive (EMC)	89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

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